AMD-K6®-2

Processor Revision Guide

Model 8

Publication # **21641** Rev: **F** Amendment/**0**
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Revision History

Date	Rev	Description
August 1998	D	Initial published release
	E	Not released
June 1999	F	Added graphic in Section 1.1 "Production Marking" to reflect the 100% laser marked package design.
June 1999	F	Added Erratum 2.3.2 "Code Segment Limit Violation Check Associated With Dual-Decoded Instructions".
June 1999	F	Added the AMD-K6-2 Model 8, CPUID Stepping C, Revision A processor
June 1999	F	Modified Section 1.1 "Production Marking" to include a 60°C OPN marking.

AMD-K6®-2 Processor Revision Guide - Model 8

The purpose of the *AMD-K6®-2 Processor Revision Guide - Model 8* is to communicate updated product information on the AMD-K6-2 processor to designers of computer systems and software developers. Model 8 of the AMD-K6-2 processor is manufactured in 0.25-micron process technology. This guide consists of four major sections:

- **Product Marking Identification:** This section provides product types, product revisions, OPNs (Ordering Part Numbers), and product marking information.
- **Product Errata:** This section provides a detailed description of product errata, including potential effects on system operation and suggested workarounds. An erratum is defined as a deviation from the product's specification.
- **Specification Changes/Clarifications:** This section provides changes, additions, and clarifications to product specifications.
- **Technical and Documentation Support:** This section provides a listing of available technical support resources. It also lists corrections, modifications, and clarifications to listed documents.

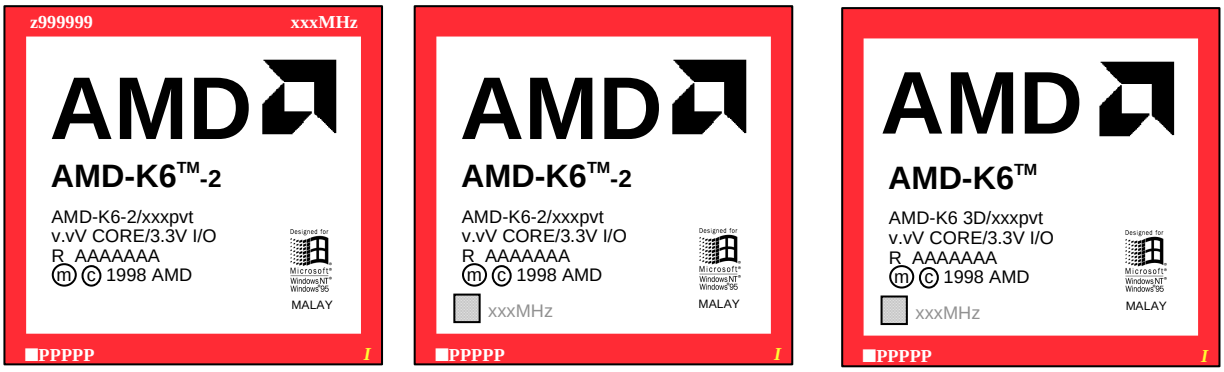
Revision Guide Policy

At times, AMD identifies deviations or changes to the specification of the AMD-K6-2 processor. These are documented in the *AMD-K6®-2 Processor Revision Guide* as errata or specification changes/clarifications and are available to anyone who requests the information. The descriptions are written to assist system and software designers in using the AMD-K6-2 processor. In addition, any corrections to AMD's published documentation on the AMD-K6 processor are included. The errata and specification changes are the result of extensive testing and validation that is done for all AMD products. AMD works closely with system and software designers to ensure the appropriate workarounds or changes are implemented to avoid impact to PC users.

The *AMD-K6®-2 Processor Revision Guide* is made publicly available to all who are interested. All issues that have been resolved and communicated to AMD's customers are included in this release.

1 Product Marking Identification

1.1 Production Marking



Ceramic Pin Grid Array (CPGA)

(Packages Not Drawn to Scale)

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xxxpvt = OPN, where:

- xxx = Operating Frequency
- p = Package Type
  - A = 321-pin PGA
- v = Operating Voltage
  - F = 2.1-2.3V Core/3.135-3.6V I/O
- t = Maximum Case Temperature
  - Q= 60°C
  - R = 70°C

v.vV = Core Voltage, where:

- 2.2V = 2.2V Component

R AAAAAAA = Revision, where:

- R = Revision
  - A = Revision A
  - B = Revision B
  - etc.
- AAAAAAA = Internally-Defined

2 Product Errata

This section documents AMD-K6-2 processor product errata. The errata are divided into categories to assist referencing particular errata. A unique tracking number for each erratum has been assigned within this document for user convenience in tracking the errata within specific revision levels. Table 2-1 cross-references the revisions of the processor to each erratum. An "X" indicates that the erratum applies to the stepping. The absence of an "X" indicates that the erratum does not apply to the stepping. Shading within the table indicates an addition or modification from the previous release of this document.

Table 2-1. Cross-Reference of Product Revision to Errata

Erratum Number	Description	CPUID Stepping[1]	
		0	C
		Revision	
		A	A
Test and Debug			
2.1.1	Boundary-Scan Test Access Port (TAP)	X	
System Bus			
2.2.1	HLDA Assertion Delayed by One Clock	X	X
2.2.2	Output Min Valid Delay Timings for 66-MHz & 60-MHz Bus Operation	X	
Interrupts and Exceptions			
2.3.1	Code Segment Limit Violation Check In Real Mode	X	
2.3.2	Code Segment Limit Violation Check Associated With Dual-Decoded Instructions	X	X
Numeric Processing			
2.4.1	Numeric Processor Status Word Not Correctly Updated	X	
2.4.2	C1 Bit of Numeric Processor Status Word	X	
Electrical Characteristics			
2.5.1	Input & Output Leakage Current	X	
	Shading indicates additions or modifications from the previous release of this document		

Notes:

1. *The CPUID stepping is returned in EAX [3:0] after executing standard function 1 of the CPUID instruction. The values shown are in hexadecimal format.*

Table 2-1. Cross-Reference of Product Revision to Errata (continued)

Erratum Number	Description	CPUID Stepping[1]	
		0	C
		Revision	
		A	A
Cache Operation			
2.6.1	Data Cache Read While NW Equals 1	X	
	Shading indicates additions or modifications from the previous release of this document		

Notes:

1. *The CPUID stepping is returned in EAX [3:0] after executing standard function 1 of the CPUID instruction. The values shown are in hexadecimal format.*

2.1 Test and Debug

2.1.1 Boundary-Scan Test Access Port (TAP)

Products Affected. CPUID Stepping 0, revision A

Normal Specified Operation. The processor supports the boundary-scan Test Access Port (TAP) as defined by the *IEEE Standard Test Access Port and Boundary-Scan Architecture (IEEE 1149.1-1990)* specification.

Non-conformance. The boundary-scan TAP is not supported.

Potential Effect on System. Boundary scan testing cannot be performed. This erratum does not affect the functional operation of a system.

Suggested Workaround. None.

Resolution Status. This erratum is corrected in the CPUID Stepping C, A revision of the AMD-K6-2 processor Model 8.

2.2 System Bus

2.2.1 HLDA Assertion Delayed by One Clock

Products Affected. CPUID Stepping 0, revision A and CPUID Stepping C, revision A

Normal Specified Operation. If $\overline{\text{BOFF}}$ and HOLD are sampled asserted on the same clock edge that negates $\overline{\text{ADS}}$, the processor asserts HLDA one clock edge after HOLD is sampled asserted.

Non-conformance. If $\overline{\text{BOFF}}$ and HOLD are sampled asserted on the same clock edge that negates $\overline{\text{ADS}}$, the processor asserts HLDA two clock edges after HOLD is sampled asserted.

Potential Effect on System. There are three potential effects of this erratum to consider:

- If the system logic asserts $\overline{\text{BOFF}}$ for a duration of one clock, anticipates the assertion of HLDA in clock 3 (see Figure 1)—which is the normal specified operation—and drives the address bus and $\overline{\text{EADS}}$ for an inquire cycle in clock 3, then the processor will not sample $\overline{\text{EADS}}$ asserted. In addition, address bus contention will occur in clock 3.
- If the system logic asserts $\overline{\text{BOFF}}$ for a duration of two clocks, anticipates the assertion of HLDA in clock 3, and drives the address bus and $\overline{\text{EADS}}$ for an inquire cycle in clock 3, then the processor will not sample $\overline{\text{EADS}}$ asserted. (No address bus contention occurs in this case.)
- If the system logic asserts $\overline{\text{BOFF}}$ for a duration of one clock, anticipates the assertion of HLDA in clock 3, and drives the address bus and $\overline{\text{EADS}}$ for an inquire cycle in clock 4, then address bus contention may occur in clock 4. (The processor will sample $\overline{\text{EADS}}$ asserted in this case.)

If the processor does not sample $\overline{\text{EADS}}$ asserted during an inquire cycle, cache/memory incoherency will occur. Address bus contention can affect the reliability of the processor and the system logic.

Suggested Workaround. The system logic must sample the assertion of HLDA before asserting $\overline{\text{EADS}}$ and driving the address bus for an inquire cycle—as shown in clock 5 of Figure 1.

Resolution Status. AMD has determined that all Socket7 and Super7™ chipsets operate as described in the aforementioned suggested workaround. Therefore, AMD has decided to defer the resolution of this erratum until deemed necessary.

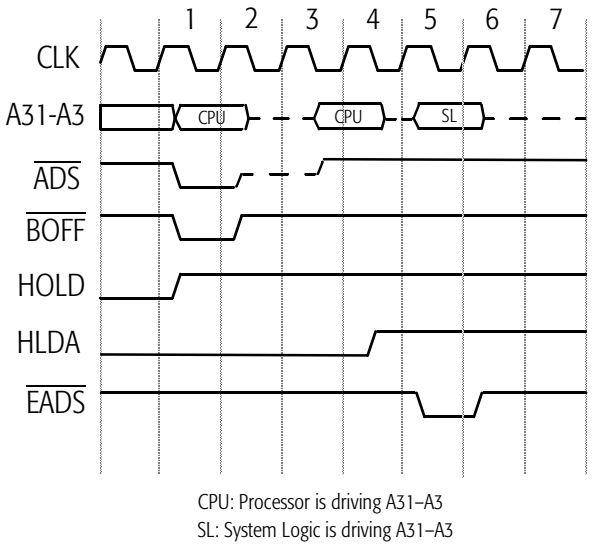

Figure 1. AMD-K6®-2 Processor Assertion of HLDA Due to Simultaneous BOFF/HOLD Assertion

2.2.2 Output Min Valid Delay Timings for 66-MHz & 60-MHz Bus Operation

Products Affected. CPUID Stepping 0, revision A

Normal Specified Operation. The minimum valid delay for all output signals is specified between 1.0 ns to 1.3 ns.

Non-conformance. The minimum valid delay for all output signals is 700 ps.

Potential Effect on System. Minimum valid delay timings directly affect hold times to the system logic. If these hold time requirements are violated, the functional operation of the system in unpredictable. This specification erratum should be fully validated on targeted system designs to ensure that all timing requirements are satisfied.

This erratum has not been observed to adversely affect system functionality.

Suggested Workaround. None.

Resolution Status. This erratum is corrected in the CPUID Stepping C, A revision of the AMD-K6-2 processor Model 8.

2.3 Interrupts and Exceptions

2.3.1 Code Segment Limit Violation Check In Real Mode

Products Affected. CPUID Stepping 0, revision A

Normal Specified Operation. When in real mode, the Instruction Pointer (IP) is compared against the code segment (CS) limit. If the IP is greater than the CS limit, a segment limit violation exception occurs.

Non-conformance. If:

- The processor is in protected mode and the CS limit is less than FFFFh
- The processor re-enters real mode by setting the PE bit in Control Register 0 (CR0) to 0 (Note: while in real mode, the CS limit defined in protected mode is still in effect)
- The target IP is greater than the limit of the code segment

Then: a segment limit violation exception does not occur, and the processor erroneously begins instruction execution starting at the address defined by the IP.

Potential Effect on System. Software that depends on the processor to generate a segment limit violation exception if the segment limit is exceeded in this particular scenario will not execute successfully. However, applications and operating systems generally do not generate segment limit violation exceptions.

It is important to note that if the target IP is less than or equal to the limit of the code segment when transferring to real mode, and the processor begins instruction execution such that the IP subsequently exceeds the limit of the code segment, then a segment limit violation exception correctly occurs.

This erratum has not been observed to adversely affect a system. It was detected by design inspection.

Suggested Workaround. Set the CS limit to FFFFh when transferring control from protected mode to real mode. This is consistent with general programming recommendations in the X86 architecture.

Resolution Status. This erratum is corrected in the CPUID Stepping C, A revision of the AMD-K6-2 processor Model 8.

2.3.2 Code Segment Limit Violation Check Associated With Dual-Decoded Instructions

Products Affected. CPUID Stepping 0, revision A and CPUID Stepping C, revision A

Normal Specified Operation. If the Extended Instruction Pointer (EIP) is greater than the code segment (CS) limit, a CS limit violation exception occurs. If the target address of a conditional branch instruction is greater than the CS limit, and the branch is not taken when this instruction is executed, then a CS limit violation exception does not occur.

Non-conformance. If Scenario 1 or Scenario 2 occurs:

Scenario 1

- Two instructions—Instruction “A” and Instruction “B”—are dual decoded by the parallel short decoders, and Instruction “A” precedes Instruction “B”

- Instruction “A” affects any of the arithmetic status flags in the EFLAGS register (CF, PF, AF, ZF, SF, or OF)
- One of the operands of Instruction “A” is a memory operand such that at least one of the following conditions is true:
  - The memory operand does not reside in the processor’s data cache
  - The page table entry (PTE) that addresses the page in which the memory operand resides does not exist in the processor’s data translation lookaside buffers (DTLBs)
- Instruction “B” is a conditional branch instruction
- One of the following conditions is true:
  - One or both of these particular instructions resides in memory above the CS limit (CS limit violation)
  - The target address of Instruction “B” is greater than the CS limit (regardless of whether the branch would be taken)

Scenario 2

- Two instructions--Instruction “A” and Instruction “B”--are dual decoded by the parallel short decoders, and Instruction “A” precedes Instruction “B”
- Instruction “A” modifies either CL or CH (general-purpose byte registers)
- Instruction “B” is a LOOP instruction and its target address is greater than the CS limit (regardless of whether the branch would be taken)

Then: the processor stalls.

Potential Effect on System. Software that contains the combination of instructions and conditions described above causes the processor to stall. However, applications and operating systems generally do not generate CS limit violation exceptions.

This erratum was detected while running software tests designed to verify the exception handling capability of the processor, and has not been observed in a system running normal software.

Suggested Workaround. Software must be written to avoid the occurrence of CS limit violations.

Resolution Status. This erratum is corrected in the CPUID Stepping 1, B revision of the AMD-K6-III processor Model 9.

2.4 Numeric Processing

2.4.1 Numeric Processor Status Word Not Correctly Updated

Products Affected. CPUID Stepping 0, revision A

Normal Specified Operation. If a numeric exception is generated by a numeric processor (NP) instruction, the NP status word is updated to reflect the results of this instruction.

Non-conformance. If:

- An NP instruction, Instruction "A," generates a numeric result exception
- An NP instruction, Instruction "B," that immediately follows Instruction "A" is speculatively executed
- Instruction "B" is aborted by the processor within the timing window that begins and ends as follows:
  - After the processor's internal microcode that handles the numeric result exception generated by Instruction "A" has commenced
  - Before this particular microcode has updated the NP status word

Then: the NP status word can be updated incorrectly following the execution of Instruction "A."

Potential Effect on System. Software that depends on the correct value of the NP status word can generate unpredictable results. This erratum was detected by design inspection and has not been observed in application or operating system software.

Suggested Workaround. None.

Resolution Status. This erratum is corrected in the CPUID Stepping C, A revision of the AMD-K6-2 processor Model 8.

2.4.2 C1 Bit of Numeric Processor Status Word

Products Affected. CPUID Stepping 0, revision A

Normal Specified Operation. The C1 bit of the numeric processor (NP) status word is affected during the execution of certain NP instructions. If a numeric result exception is generated by any of these particular NP instructions, the state of the C1 bit remains unchanged.

Non-conformance. If:

- The C1 bit of the NP status word is set to 1 during the execution of an NP instruction, Instruction "A"
- Instruction "A" generates a numeric result exception
- The numeric processor speculatively executes an NP instruction, Instruction "B," that clears the C1 bit (C1 equals 0)
- Instruction "B" is aborted by the processor

Then: the C1 bit of the NP status word may remain set to 0 following the execution of Instruction "A."

Potential Effect on System. If:

- The C1 bit is not affected by the processor's internal microcode that handles the numeric result exception generated by Instruction "A"
- The next NP instruction, Instruction "C", does not clear the C1 bit, and this instruction depends on the state of the C1 bit

Then: the results of Instruction "C" can be incorrect.

This erratum was detected by design inspection and has not been observed in application or operating system software. To date, the only known method for generating this erratum is to execute a FPREM or FPREM1 instruction that generates a denormal result with the C1 bit set to 1, followed by executing the FSTSW instruction, which would erroneously return a value of 0 for the C1 bit.

Suggested Workaround. None.

Resolution Status. This erratum is corrected in the CPUID Stepping C, A revision of the AMD-K6-2 processor Model 8.

2.5 Electrical Characteristics

2.5.1 Input & Output Leakage Current

Products Affected. CPUID Stepping 0, revision A

Normal Specified Operation. The maximum input (I_{LI}) and output leakage (I_{LO}) current is specified as +/-15µA.

Non-conformance. The maximum input (I_{LI}) and output leakage (I_{LO}) current is +200µA/-250µA.

Potential Effect on System. The outline below lists the potential effects on a system due to excessive negative and positive leakage. This specification erratum should be fully validated on targeted system designs to ensure functional operation.

Excessive negative leakage current may…

- for I/O pins with weak pull-downs, cause intended Low signals to be detected above Input Low Voltage thresholds (V_{IL} = 0.8V).
- slightly increase the signal fall-time and slightly decrease the signal rise-time.
- increase in-circuit test delays for a High driven, pull-down pin to reach a safe Low voltage level when Tri-stated.
- slightly increase the power consumption for I/O pins with external pull-down resistors (greater impact in low-power states).

Excessive positive leakage current may…

- for I/O pins with weak pull-ups, cause intended High signals to be detected below Input High Voltage thresholds (V_{IH} = 2.0V).
- slightly increase the signal rise-time and slightly decrease the signal fall-time.
- increase in-circuit test delays for a Low driven, pull-up pin to reach a safe High voltage level when Tri-stated.
- slightly increase the power consumption for I/O pins with external pull-up resistors (greater impact in low-power states).

Identifying processor Input pins, critical by design, with weak pull-up or pull-down resistors and limiting the amount of leakage current allowed on these pins ensures signal voltage levels do not drift above V_{IL} or below V_{IH} levels due to leakage current. Subsequent to the +200µA/-250µA production test on I/O pins, AMD has implemented a tighter test to screen Input pins potentially affected by this erratum. Validating, through system tests, that signal timings remain within system logic and processor requirements ensures signal timings are not adversely affected by leakage current.

This erratum has not been observed to adversely affect system functionality.

Suggested Workaround. None.

Resolution Status. This erratum is corrected in the CPUID Stepping C, A revision of the AMD-K6-2 processor Model 8.

2.6 Cache Operation

2.6.1 Data Cache Read While NW Equals 1

Products Affected. CPUID Stepping 0, revision A

Normal Specified Operation. If the Not Writethrough (NW) bit of Control Register 0 (CR0) is set to 1, write hits update the processor's Level-1 (L1) cache, but do not update external memory. Write misses update external memory, and do not cause cache-line allocations to occur. In either event, the correct physical memory location is updated accordingly.

Non-conformance. If:

- The software has defined the page tables such that two linear addresses (LA1 and LA2) map to the same physical page, but LA1[13:12] does not equal LA2[13:12]
- The processor allocates and loads a cache line that maps to one of these linear addresses, LA1, and this cache line is marked *shared* (either during the cache line fill, or by an inquire cycle that occurs after the cache line fill)
- The Not Writethrough (NW) bit of Control Register 0 (CR0) is then set to 1
- The processor detects a write hit to this particular shared line using the other linear address, LA2

Then: the processor writes data to a different cache line that corresponds to a different physical address than the address mapped to LA2.

Potential Effect on System. This erratum does not affect normal operation because the NW bit is set to 0 for normal operation. However, if NW is set to 1 and this erratum occurs, reads from the cache may return incorrect data.

This erratum was detected by design inspection and has not been observed in application or operating system software.

Suggested Workaround. Do not set the NW bit to 1. If the NW bit must be set to 1, then this erratum can be avoided in several ways:

- Flush the L1 cache prior to setting the NW bit to 1
- Avoid using linear addresses that map to the same physical page, but differ in bits 12 and 13
- Avoid marking cache lines to the shared state

Resolution Status. This erratum is corrected in the CPUID Stepping C, A revision of the AMD-K6-2 processor Model 8.

3 Specification Changes/Clarifications

This section documents AMD-K6-2 processor specification changes and clarifications. The changes/clarifications are divided into categories to assist referencing particular changes. A unique tracking number for each change/clarification has been assigned within this document for user convenience in tracking the specification change/clarification within specific revision levels. Table 3-2 cross-references the revisions of the processor to each specification change/clarification. An "X" indicates that the specification change/clarification applies to the stepping. The absence of an "X" indicates the specification change/clarification does not apply to the stepping.

Table 3-2. Cross-Reference of Product Revision to Specification Change/Clarification

Change Number	Description	CPUID Stepping[1]	
		0	C
		Revision	
		A	A
Interrupts and Exceptions			
3.1.1	Recognition of External Hardware Interrupts During I/O Read Cycle	X	X
Instructions			
3.2.1	SYSCALL and SYSRET	X	X
Ordering Information			
3.3.1	Valid Ordering Part Number Combinations	X	X
	Shading indicates additions or modifications from the previous release of this document		

Notes:

1. The CPUID stepping is returned in EAX [3:0] after executing standard function 1 of the CPUID instruction. The values shown are in hexadecimal format.

3.1 Interrupts and Exceptions

3.1.1 Recognition of External Hardware Interrupts During I/O Read Cycle

New Specification Applies to: CPUID Steppings 0 and C, all revisions

Previous Operation. For I/O Reads, the AMD-K6-2 processor waits for preceding instructions to complete before executing the I/O Read instruction. However, there is no serialization for succeeding instructions. This means that succeeding instructions can be executed in parallel with the I/O Read. As a result, external interrupts may not be recognized and serviced before succeeding instructions are completed.

New Operation. For I/O Reads, the AMD-K6-2 processor waits for preceding instructions to complete before executing the I/O Read instruction and it serializes succeeding instructions. This means that the I/O Read instruction completes before any succeeding instructions are executed. Such serialization allows for external interrupts, asserted during the I/O cycle, to be recognized and serviced before any dependent instructions are executed.

Implication. The previous and new operation has no implication for software and hardware that are designed to the Socket 7 specification, which states that IN instructions are not fully serialized.

3.2 Instructions

3.2.1 SYSCALL and SYSRET

New Specification Applies to: CPUID Steppings 0 and C, all revisions

Previous Operation. The AMD-K6-2 processor supports the SYSCALL and SYSRET Extensions, which provide a fast method for entering and exiting an operating system. Bit 10 of the Extended Feature Flags (Function 8000_0001h of the CPUID instruction) is set to 1 to indicate support for the SYSCALL and SYSRET Extensions. Bit 11 of the Extended Feature Flags is Reserved.

New Operation. Bit 11 of the Extended Feature Flags indicates whether support for the SYSCALL and SYSRET Extensions exists—if bit 11 is set to 1, then the SYSCALL and SYSRET Extensions are supported; if bit 11 is set to 0, then the SYSCALL and SYSRET Extensions are not supported.

Implication. Since no operating systems currently utilize these instructions, there is no implication to existing software. For the future, the Extended Feature flags must be read and interpreted as defined in *New Operation* in order to determine if a specific stepping of the AMD-K6-2 processor supports the SYSCALL and SYSRET Extensions.

3.3 Ordering Information

3.3.1 Valid Ordering Part Number Combinations

New Specification Applies to: CPUID Steppings 0 and C, all revisions

Previous Operation. Table 3-3 contains the valid Ordering Part Number (OPN) combinations of the AMD-K6-2 processor Model 8.

Table 3-3. Previous Specified Valid Ordering Part Number Combinations

OPN	Package Type	Operating Voltage	Case Temperature
AMD-K6 3D/333AFR	321-Pin CPGA	2.1V-2.3V (Core) 3.135V-3.6V (I/O)	0°C-70°C
AMD-K6 3D/300AFR	321-Pin CPGA	2.1V-2.3V (Core) 3.135V-3.6V (I/O)	0°C-70°C
AMD-K6 3D/266AFR	321-Pin CPGA	2.1V-2.3V (Core) 3.135V-3.6V (I/O)	0°C-70°C
AMD-K6 3D/250AFR	321-Pin CPGA	2.1V-2.3V (Core) 3.135V-3.6V (I/O)	0°C-70°C
AMD-K6 3D/233AFR	321-Pin CPGA	2.1V-2.3V (Core) 3.135V-3.6V (I/O)	0°C-70°C

New Operation. Table 3-4 contains the valid Ordering Part Number (OPN) combinations of the AMD-K6-2 processor Model 8.

Table 3-4. New Specified Valid Ordering Part Number Combinations

OPN	Package Type	Operating Voltage	Case Temperature
AMD-K6-2/475AHX	321-Pin CPGA	2.3V-2.5V (Core) 3.135V-3.6V (I/O)	0°C-65°C
AMD-K6-2/450AHX	321-Pin CPGA	2.3V-2.5V (Core) 3.135V-3.6V (I/O)	0°C-65°C
AMD-K6-2/400AFQ	321-Pin CPGA	2.1V-2.3V (Core) 3.135V-3.6V (I/O)	0°C-60°C
AMD-K6-2/380AFR	321-Pin CPGA	2.1V-2.3V (Core) 3.135V-3.6V (I/O)	0°C-70°C
AMD-K6-2/366AFR	321-Pin CPGA	2.1V-2.3V (Core) 3.135V-3.6V (I/O)	0°C-70°C
AMD-K6-2/350AFR	321-Pin CPGA	2.1V-2.3V (Core) 3.135V-3.6V (I/O)	0°C-70°C
AMD-K6-2/333AFR	321-Pin CPGA	2.1V-2.3V (Core) 3.135V-3.6V (I/O)	0°C-70°C

Table 3-4. New Specified Valid Ordering Part Number Combinations

OPN	Package Type	Operating Voltage	Case Temperature
AMD-K6-2/300AFR	321-Pin CPGA	2.1V-2.3V (Core) 3.135V-3.6V (I/O)	0°C-70°C
AMD-K6-2/266AFR	321-Pin CPGA	2.1V-2.3V (Core) 3.135V-3.6V (I/O)	0°C-70°C
AMD-K6-2/233AFR	321-Pin CPGA	2.1V-2.3V (Core) 3.135V-3.6V (I/O)	0°C-70°C

Implication. The package marking is changed to reflect the new specified OPN. The new package marking is illustrated in Section 1, “Product Marking Identification”, on page 2.

4 Technical and Documentation Support

4.1 Documentation Support

The following documents provide additional information regarding the operation of the AMD-K6-2 processor:

- AMD-K6®-2 Processor Data Sheet (order# 21850)
- 3DNow!™ Technology Manual (order# 21928)
- AMD-K6®-2 Processor Code Optimization Application Note (order# 21924)
- AMD-K6® Processor Multimedia Technology Manual (order# 20726)
- AMD K86™ Family BIOS and Software Tools Developers Guide (order# 21062)
- AMD-K6® Processor BIOS Design Application Note (order# 21329)
- AMD Processor Recognition Application Note (order# 20734)
- Implementation of Write Allocate in the K86™ Processors (order# 21326)
- AMD-K6® Processor Thermal Solution Design Application Note (order# 21085)
- AMD-K6® Processor Power Supply Design Application Note (order# 21103)
- AMD-K6® Processor I/O Model Application Note (order# 21084)
- AMD-K6® Processor V_{CC2} Voltage Detection Application Note (order# 21635)
- SYSCALL and SYSRET Instruction Specification Application Note (order# 21086)
- AMD-K6® Processor x86 Code Optimization Application Note (order# 21828)
- AMD-K6® Processor 100-MHz Bus Specification Application Note (order# 21644)
- AMD-K6® Processor EMI Design Considerations Application Note (order# 22023)

For the latest updates, refer to www.amd.com/K6/k6docs and download the appropriate files.